Proposal for IEC 62700 Identification and Communication Method for Notebook Computer supporting Class 1-3 ID

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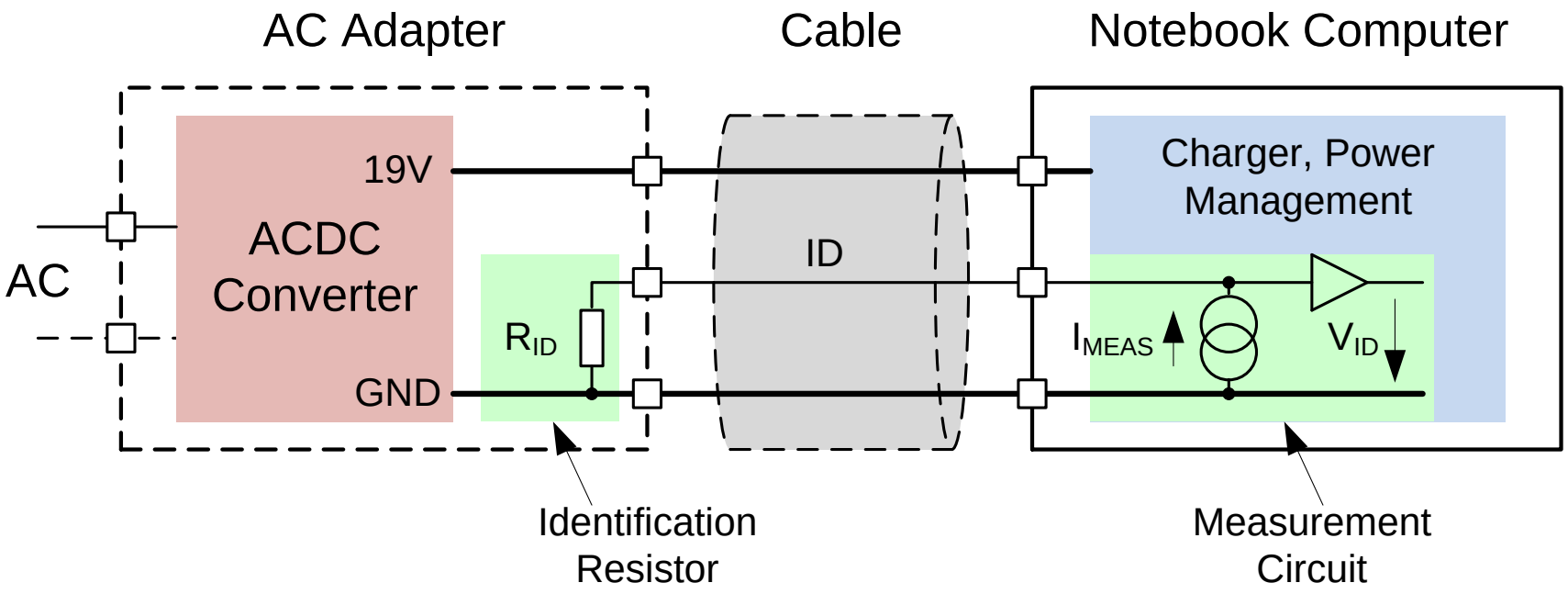
Overview

- IEC62700 Requirements
- Low Cost Adapter Identification
- Smart Adapter Identification
- Communication Protocol
- References

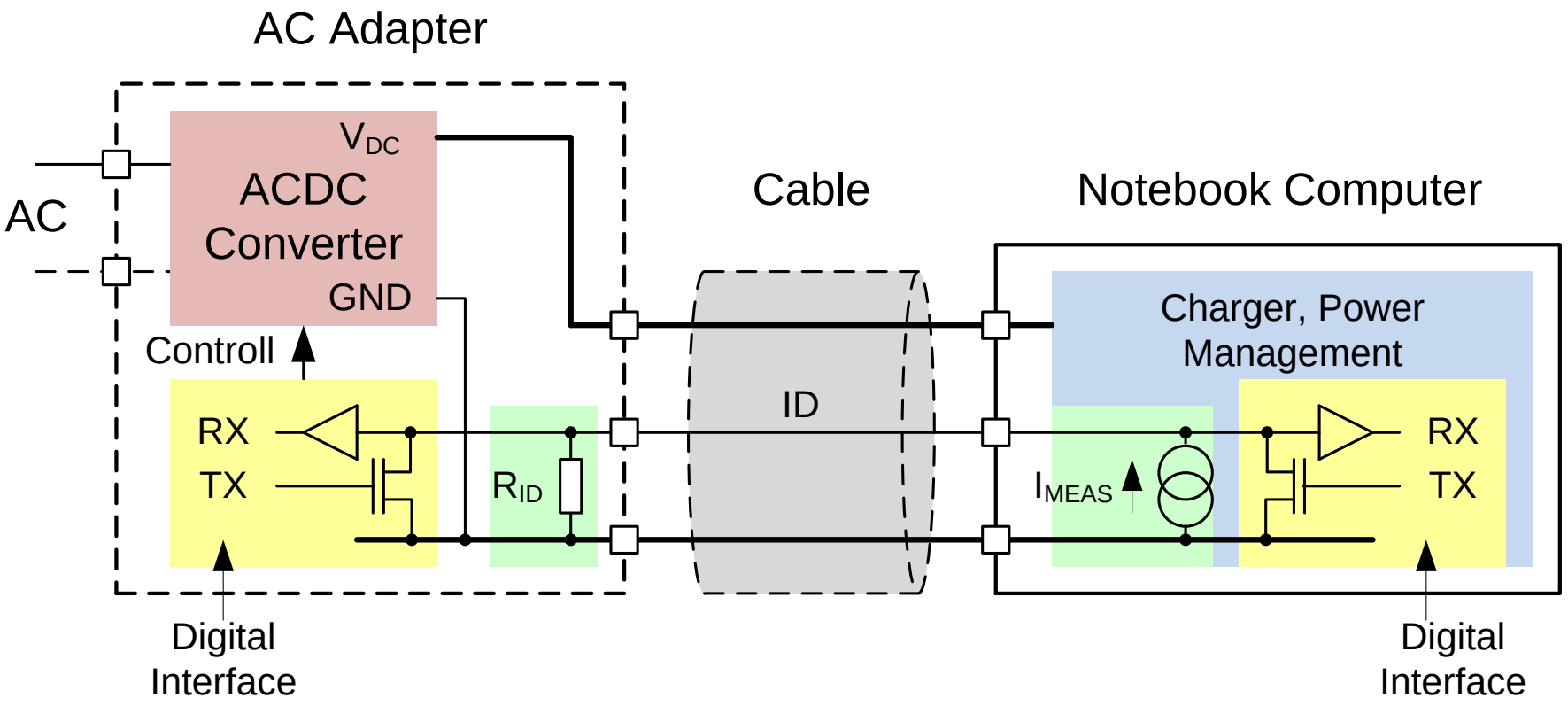
IEC62700 – Communication Protocol related Questions

- Is **ID PIN communication mandatory** for functionality?
- When should it be acceptable for a computer to reject certain models of AC adapter?
- What **communications standard** to use?
- What should the system do in the event of a failure of the communications?
- Can a scalable system of both **low cost analog and higher function digital** approaches be devised?
- Should communication be **bidirectional**, or support networking of multiple devices?
- What is the **minimum information** that shall be provided by the AC adapter?
- What obligations does the Notebook Computer have to the AC adapter?
- What mechanism will allow for OEM specific innovation? To gain acceptance the Technical Specification should not exclude innovative or **proprietary solutions from manufacturers**.
- What roadmap can be provided for future **innovation in communication** method, or what process can be used for **standardizing new data**?

Identification for Low Cost Adapter



Identification for „Smart Adapter“

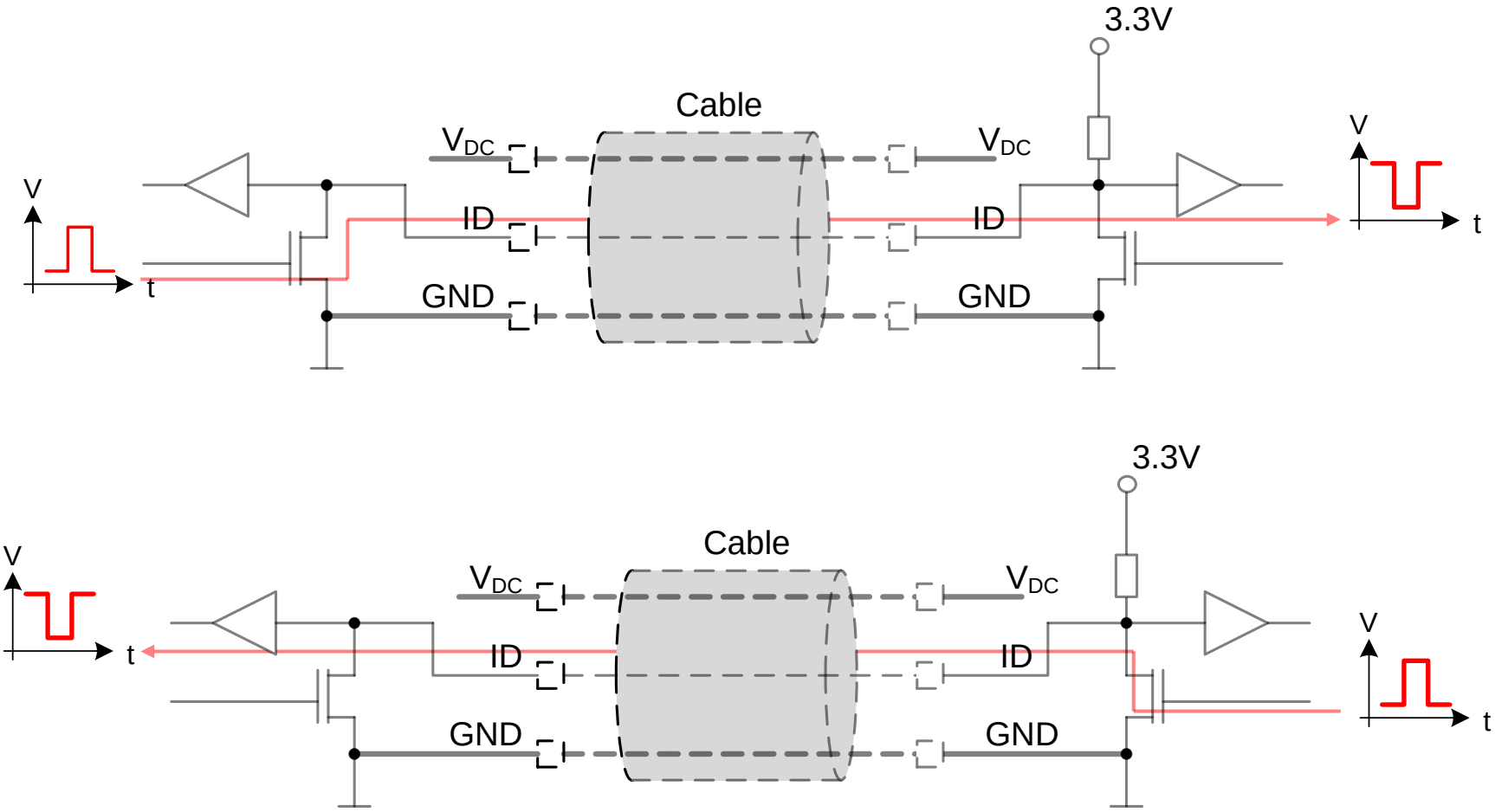


Adapter Identification

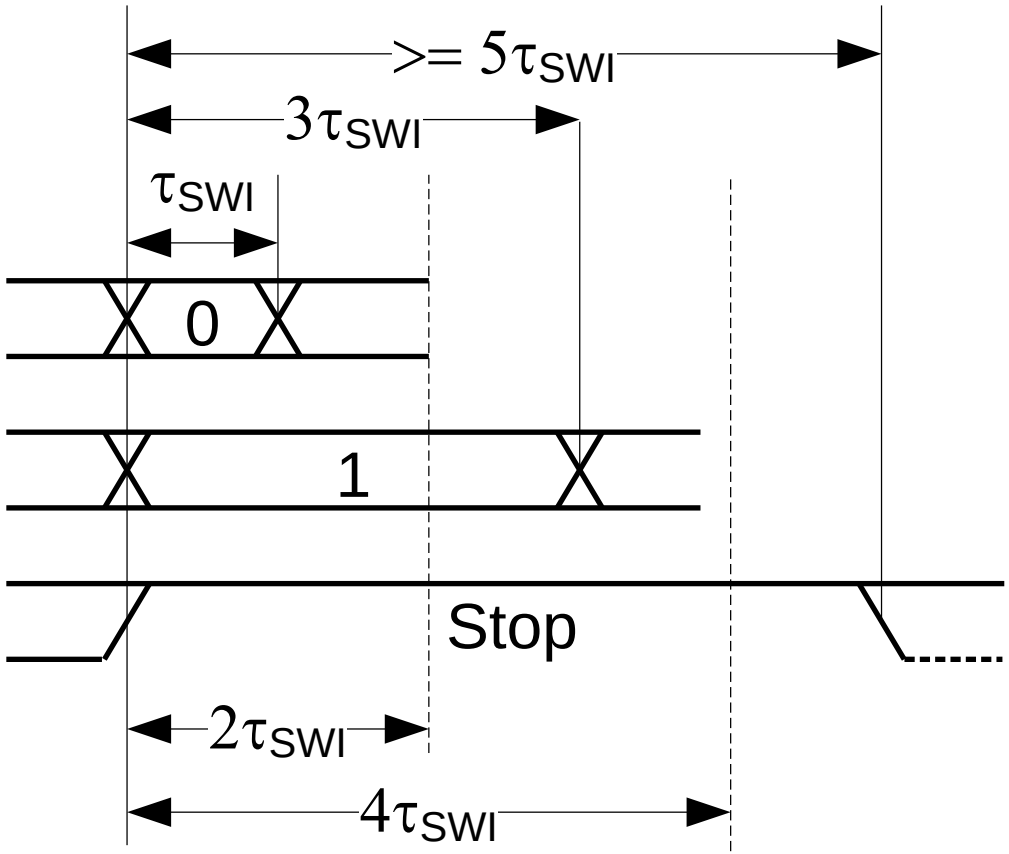
R_{ID}	Adapter Type	Value
>750 KΩ	No Adapter present	
330 KΩ ±30%	Smart Adapter	→ Digital Identification
180 KΩ ±5%	Low Cost Adapter	Power Class 0
120 KΩ ±5%		Power Class 1
82 KΩ ±5%		Power Class 2
56 KΩ ±5%		Power Class 3
39 KΩ ±5%		Power Class 4

Resistor values chosen from IEC60063 E12 series

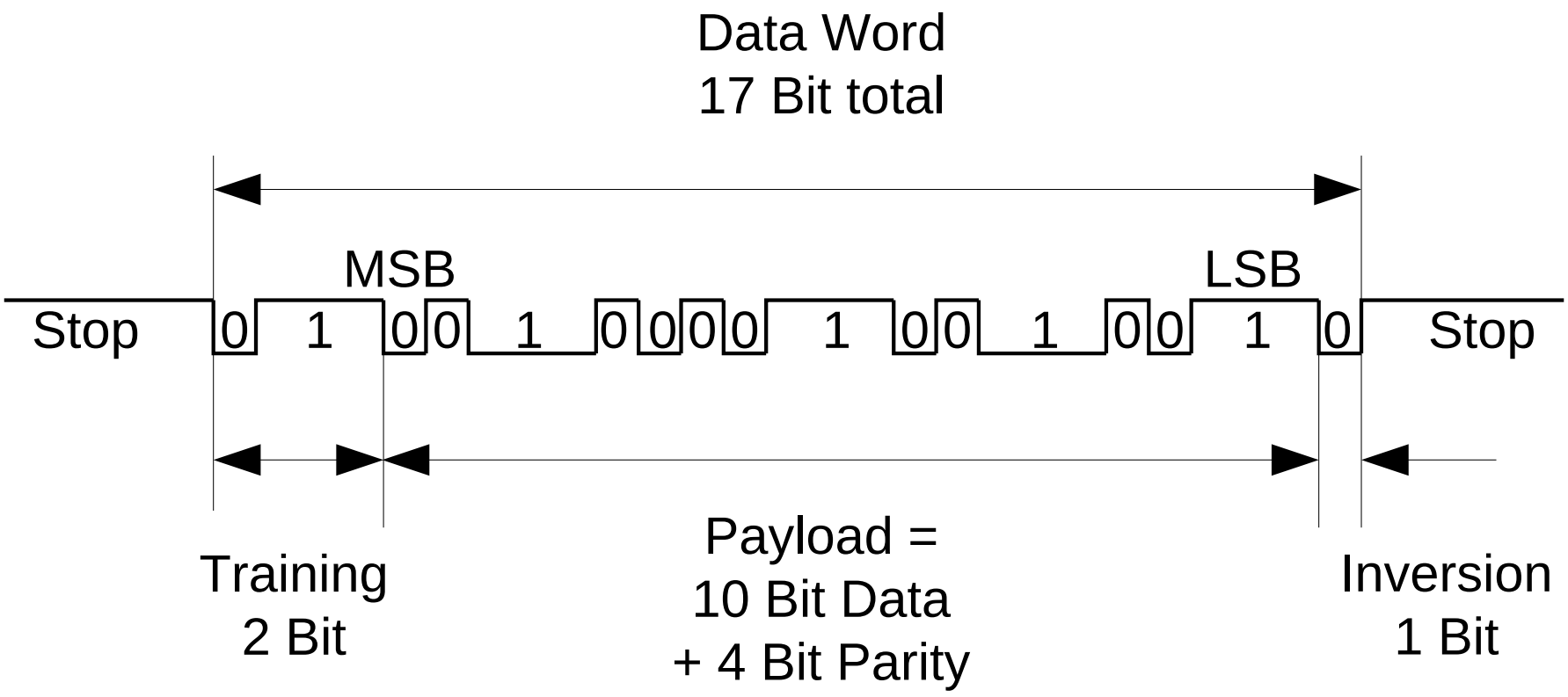
Bidirectional Communication



Infineon Single Wire Interface (SWI)
Time Distance Coding

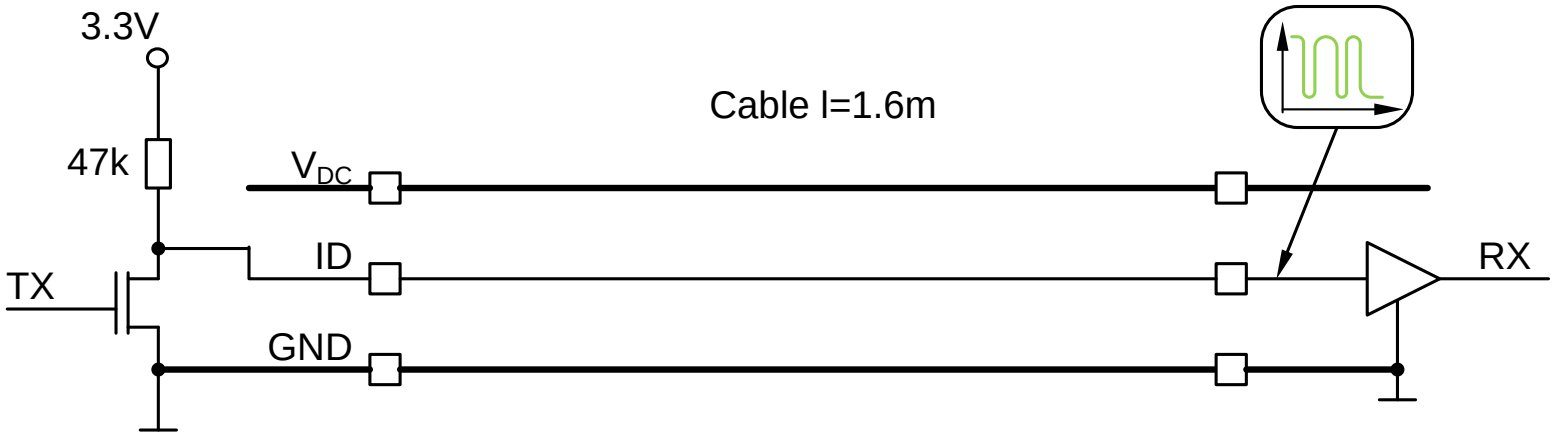


SWI Data Word



MSB = Most Significant Bit
LSB = Least Significant Bit

Practical Performance Demo



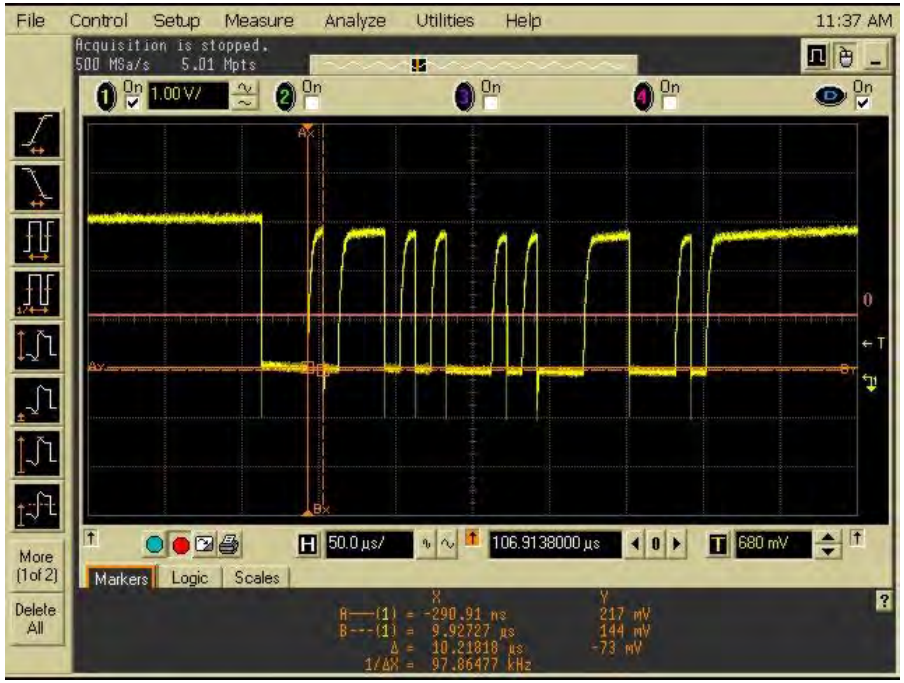
V_{PU} = 3.3V

τ_{SWI} = 10µs

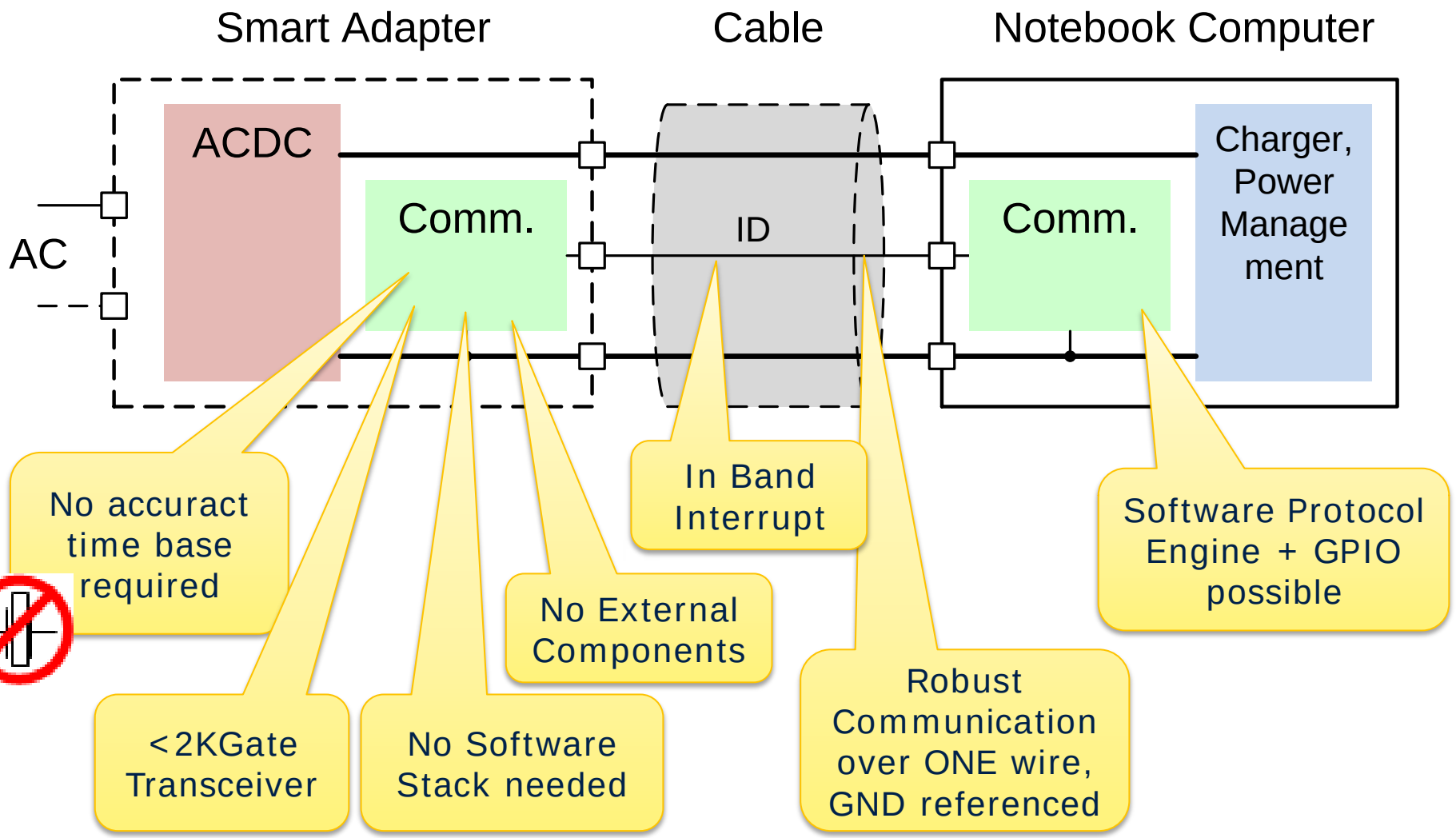
50KBit/s peak

R_{PU}=47k

1.60m cable



Merits of Infineon Single Wire Interface

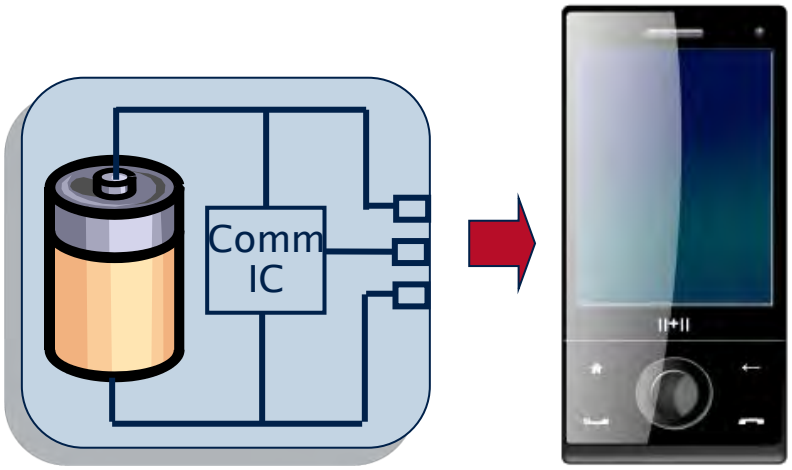


“Smart” Functions

- Identification of Adapter
  Vendor, Product Number, Serial Number, …
- Query Adapter Capabilities
  Power Class, Output Voltages, Current Supply Capabilities, …
- Cryptographic Authentication of Adapter
- Adapter Output Voltage and Current Control
- Telemetry of Adapter Parameters
  Temperature (Know thermal shut-down in advance), AC Voltage, Output Voltage, Output Current, Instantaneous Power

SWI used in MIPI ® Battery Interface

- Digital Battery Interface for mobile phones/terminals
  - Efficiently charging modern batteries
  - Authentication
  - Sensors inside battery
- Infineon **Single Wire Interface** used as Link Layer
- Final BIF standard V1.0 released by MIPI board Feb. 2012, Presented at World Mobile Congress 2012
- V1.1 to be released in June 2014
- Implemented in most Smart Phone / Tablet chipsets



mipi alliance

http://www.mipi.org/specifications/battery-interface

SWI Resources

- SWI related Patents
  - Communication Protocol - US7636806
  - Device Discovery Mechanism - US8099469
  - Master PHY Circuit - US20120105051

- IFX Products using SWI / MIPI BIF
  - Battery Authentication Origa™

ENERGY EFFICIENCY
MOBILITY
SECURITY

Innovative semiconductor solutions for energy efficiency, mobility and security.



Communication Interface Comparison

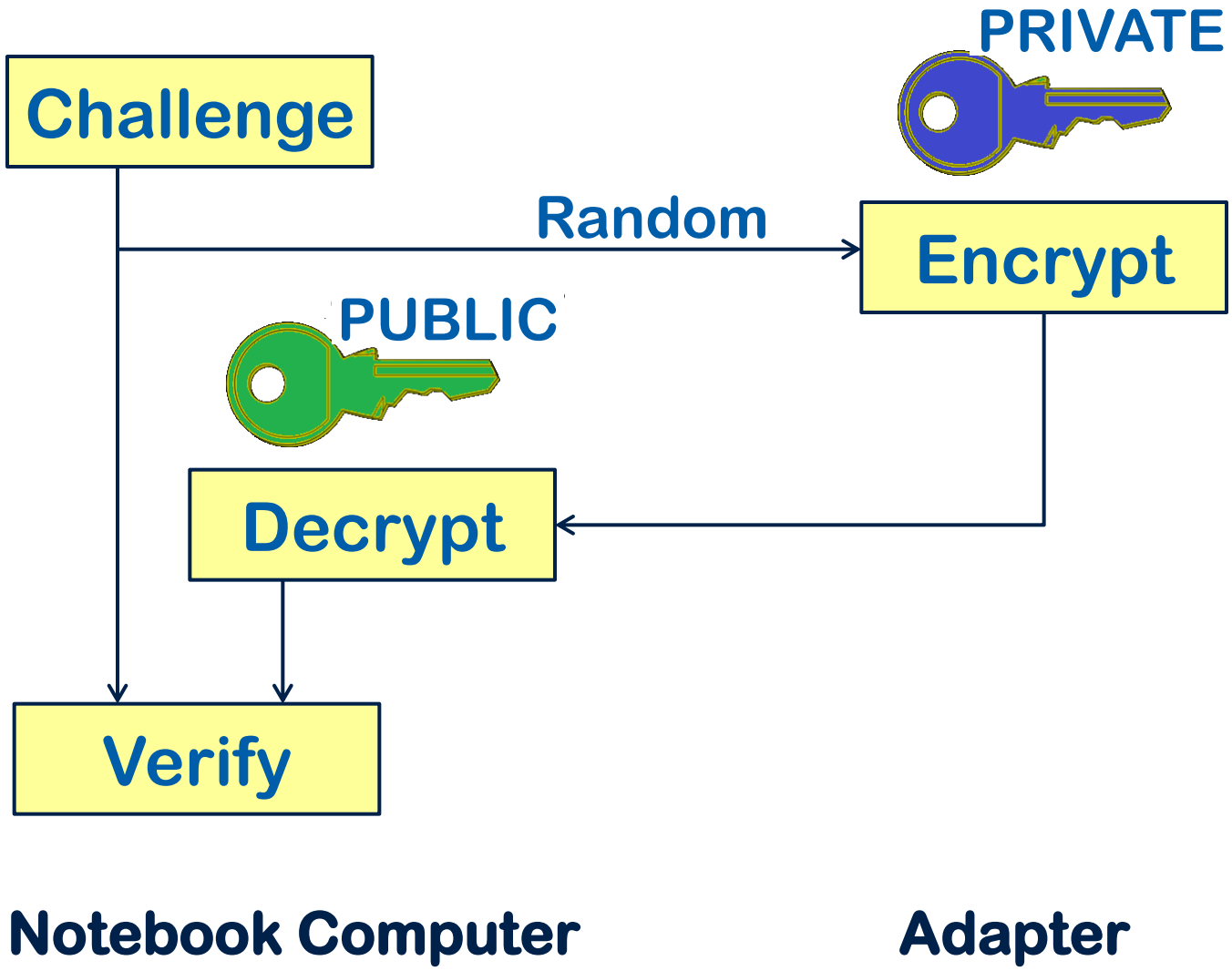
	SWI	PLC*	I2C /PMBUS	UART
# of Comm. Wires	1	0	2	1/2
<2KGate RXTX	YES	NO	YES	YES
±30% Slave Clock	YES	NO	YES	NO
HW only Slave	YES	NO	YES	YES
In-band Interrupt	YES	NO	NO	NO
SW only Master	YES	NO	YES	YES
External Components	Non	LC - Filter	Non	Non
Robustness	High	High	Not for Wire!	Medium

* Power Line Communication, FSK (Frequency Shift Keying)

Other Features of SWI

- Remote Powering of Adapter for Wakeup
- Strong Error Protection with Hamming Parity
- Flexible Data Rate up to 500kBit/s
  - Slow speed for 32.768kHz Host Operation
  - High Speed for fast Authentication
  - Adaptive speed depending on cable length
- Multiple Slaves supported
- Device Discovery Mechanism
- Customizable Address space (e.g. 64K x 8 Byte)
- Vendor specific Extensions supported

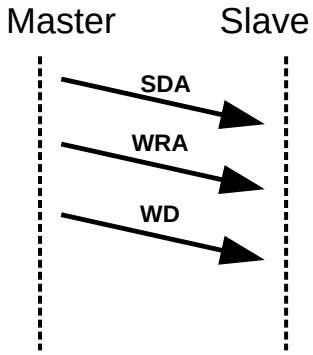
Authentication



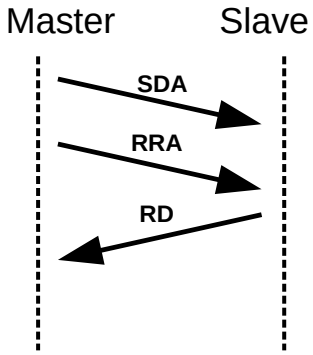
SWI Bus Transactions Elements

Direction	Word	Code	BCF	Bit #9	Bit #8	Bit #7..#0	Response
Master to all Slaves (Broadcast)	Bus Command	BC	1_B	0_B	0_B	Command	1)
	Extended Device Address	EDA	1_B	0_B	1_B	Device address (high)	-
	Slave Device Address	SDA	1_B	1_B	0_B	Device address (low)	-
	Master Device Address	MDA	1_B	1_B	1_B	Device address low	-
Master to active Slave(s) (Multicast)	Write Data	WD	0_B	0_B	0_B	Write data	-
	Extended Register Address	ERA	0_B	0_B	1_B	Register address (high)	-
	Write Register Address	WRA	0_B	1_B	0_B	Register address (low)	-
	Read Register Address	RRA	0_B	1_B	1_B	Register address low	RD
Slave to active Master (Unicast)	Read Data	RD	0_B	ACK	EOT	Read data / error code	-

SWI Bus Transactions



8 Bit Write to 8 Bit Address Space with Device Adressing



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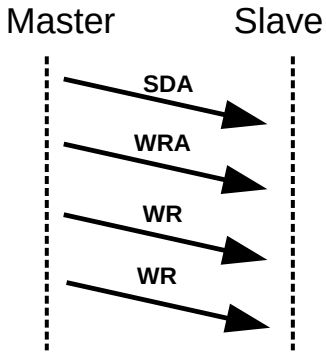
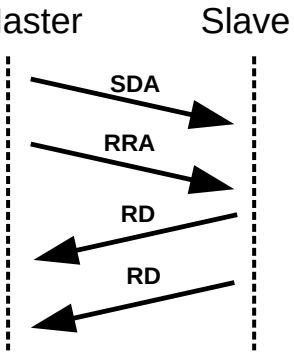
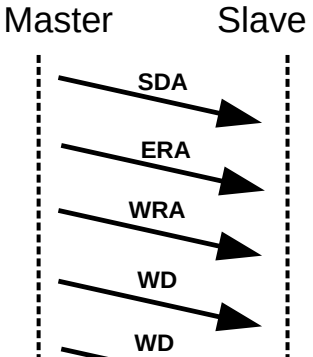


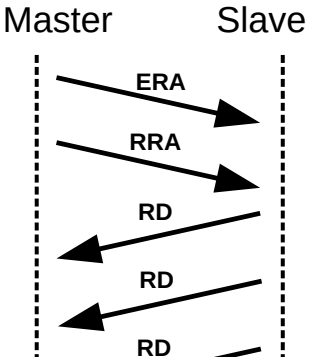
16 Bit Write to 8 Bit Address Space with Device Adressing



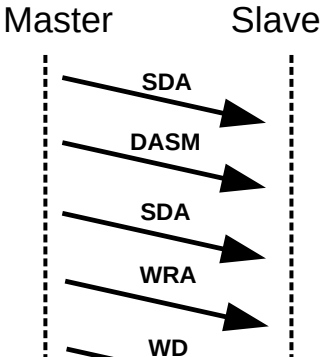
16 Bit Read from 8 Bit Address Space with Device Adressing



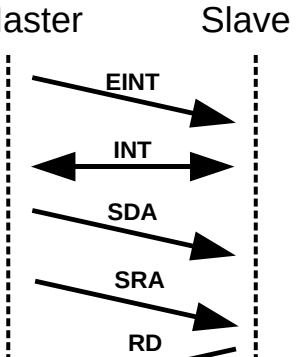
16 Bit Write to 16 Bit Address Space with Device Adressing



32 Bit Read from 16 Bit Address Space



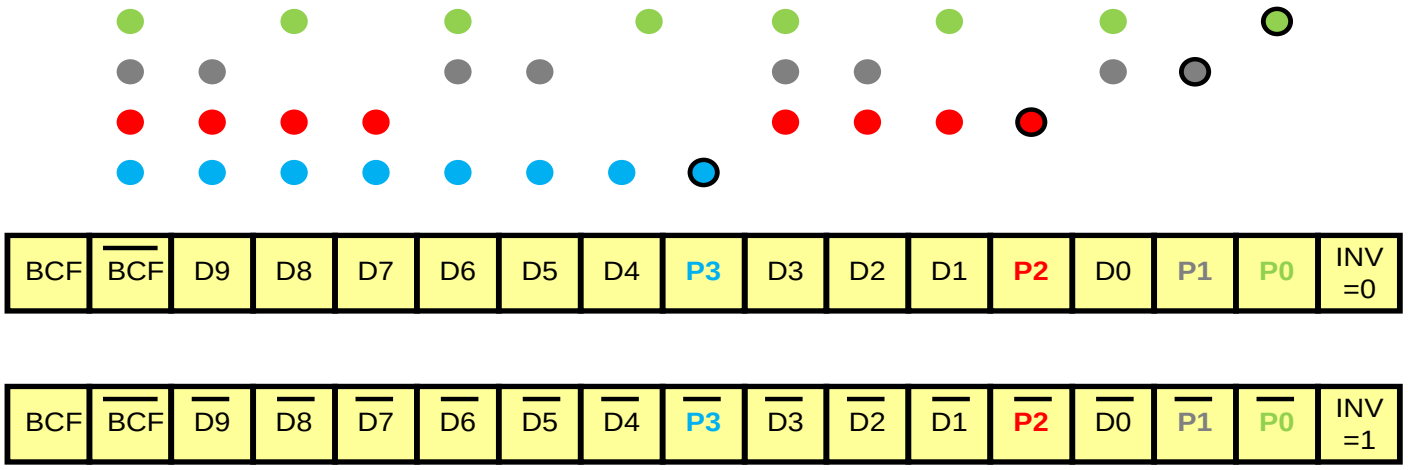
8 Bit Write to 8 Bit Address Space with two Slave devices Addressed



Bus Interrupt with following 8 Bit Read 8 Bit Address Space

SWI_Transactions.vsd

SWI Error Protection



SWIDataProtection.vsd

- 15 bit Hamming Code (11 bit payload, 4 bit parity)
  - Repair 1-bit errors
  - Detect multi-bit errors

SWI Master PHY Circuit (Example)